Performance Comparison of CNFET-Based (8:2) and (8:3) Compressors

Shima Mehrabi
Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran
Email: sh.mehrabi@srbiau.ac.ir

Amirhossein Jamalian
Artificial Intelligence, Faculty of Computer Science, Technical University of Chemnitz, Germany
Email: amj@hrz.tu-chemnitz.de

***Abstract*— Compressors are known as a key processing elements to accumulate and reduce partial products in a parallel manner in multipliers. This paper conducts a comprehensive analysis and comparison between two high-order (8:2) and (8:3) compressors based on Carbon Nanotube Field Effect Transistor (CNFET) technology. Furthermore, two well-known Full-Adder (FA) are also employed within the cells to analyse and compared for speed, power consumption, and power-delay product at transistor-level.**

Simulations are carried out using Synopsys HSPICE with 32nm CNTFET technology.The results of simulation demonstrate the superiority of the (8:3) compressor in terms of power and Power-Delay Product (PDP) around 67% and 44% respectively in comparison with (8:2) compressors by deploying symmetrical CNT Full-Adder cells.

***Index Terms*— Full-Adder, Compressor, Multiplier, Low-Power, High-performance, CNFETs, Nanotechnology**

I. Introduction

Arithmetic Logic Unit (ALU) is known as a fundamental building block of many types of computing circuits and arithmetic circuits are a natural model for computing arithmetic functions such as multiplying, adding , shifting and etc [1-2]. Since, in today's VLSI (Very Large Scale System Integrated) circuit design, improving the design of high-performance, low-power proceesing elements are desired, computing circuits such as multipliers and adders are concerned in digital circuit design. Moreover, doing things fast requires more logic and thus more space. Multipliers play an effective role in in many error-tolerant applications such as digital /image signal processing [3-4]. Moreover, they are known as the fundamental computational unit in microprocessors and microprocesors are the heart of every digital device from smart phone and tablets to large computers and servers[5-6].

Compressors and counters considered as the crucial component of each multiplier block. They are usually composed of cascaded single-bit adder blocks[7] So, high-speed, low-power compressors are highly desired to have high performance multipliers.

A compressor is simply an adder circuit. They are known as the basic unit of multipliers and multipliers are considered as the fundamental unit of each microprocessors, embedded systems and crypto processors [8-9]. In this paper, we analyze two high-order (8:2) and (8:3) compressors in transistor-level. Two recent CNTFET-based Full-Adder cells designs are utilized to evaluate and compare the performance of these two compressors.

The rest of the paper is organized as follows: in section *II*, conventional design and architecture of (8:2) and (8:3) compressors are reviewed. Section *III*, include implementation of these two compressors by employing the two recent CNT-based Full-Adder circuit design and experimental results, analyses and comparisons are presented and section *IV* concludes the paper.

II. Conventional Architecture of High-order (8:2) and (8:3) Compressors

Compressors are simple circuits that reduce a large number of equal-value inputs to a smaller number of outputs by adding the inputs and producing some outputs with higher value. A typical (m:n) compressor takes *m* equally weighted input bits and produces *n*-bit binary number [6]. Moreover, there is a strong connection between compressors and Adders because The internal architecture of compressors show that compressors composed of some cascade adders.

A. High-order (8:2) Compressor

The block diagram of conventional (8:2) compressors [10] consist of six cascaded Full-Adder cells, according to Fig.1. So the critical path of (8:2) compressor consists of four Full-Adder cells.

As it depicted, the high-order (8:2) compressors have three extra inputs (Cin) and three extra outputs (Cout) as carry signals. As it is lucid in (1), the total output weights equal 11×2^k including the inputs/outputs carry signals so the overhead is not negligible.

Manuscript received July 24, 2018; revised May 24, 2019.

doi: 10.18178/ijmerr.8.4.536-541

$$\sum \text{Input Weights} = \sum \text{Output Weights} \quad (1)$$
$$11*2^{K} = 2^{K} + 2^{K+1} + 2^{K+1} + 2^{K+1} + 2^{K+2}$$
$$11*2^{K} = 11*2^{K}$$

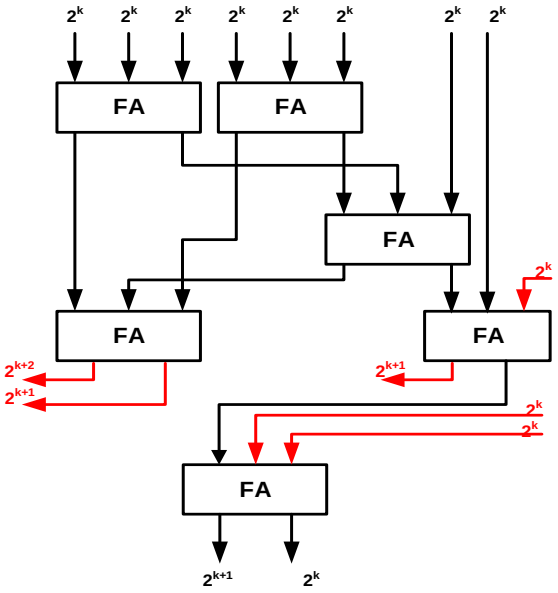


Figure 1. Block diagram of the conventional (8:2) compressor

B. High-order (8:3) Compressor

According to Fig.2, the inner structure of conventional (8:3) compressors [11-13] consist of five Full-Adder cells with two Half-Adder which are cascaded. So the critical path of (8:3) consists of three Full-Adder and one Half-Adder cells. Obviously, the (8:3) compressor have the better critical path to compare with (8:2) compressor.

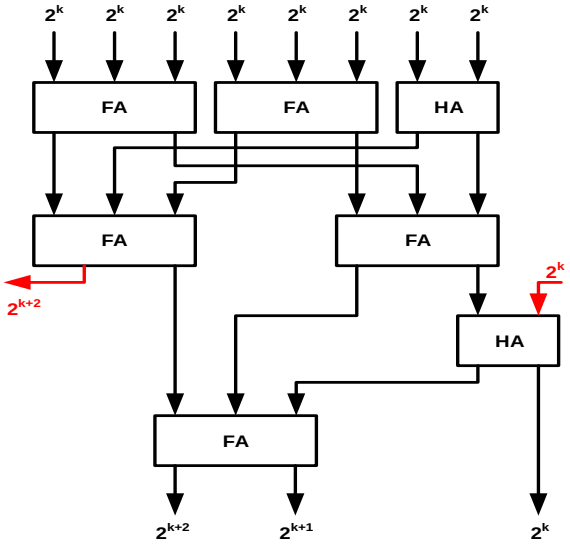


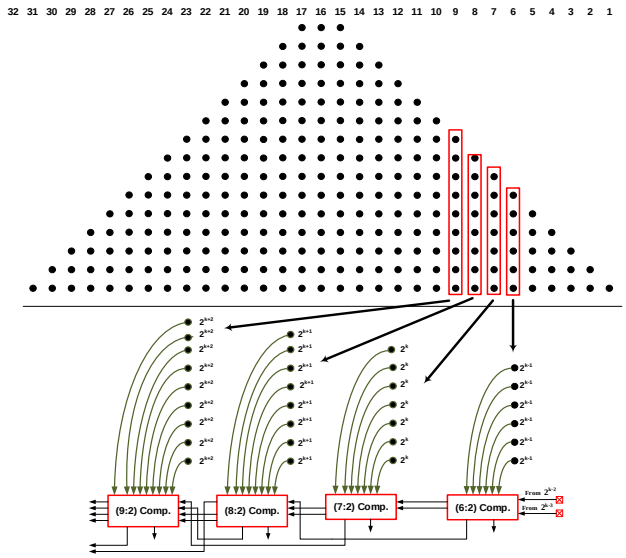
Figure 2. Block diagram of the conventional (8:3) compressor

Moreover, the high-order (8:3) compressors have higher compression efficiency paying the price of one extra inputs (Cin) and one extra outputs (Cout) as carry signals. In (2), the total output weights equal 9×2^{k} including the only one input/output carry signal so the overhead is negligible.

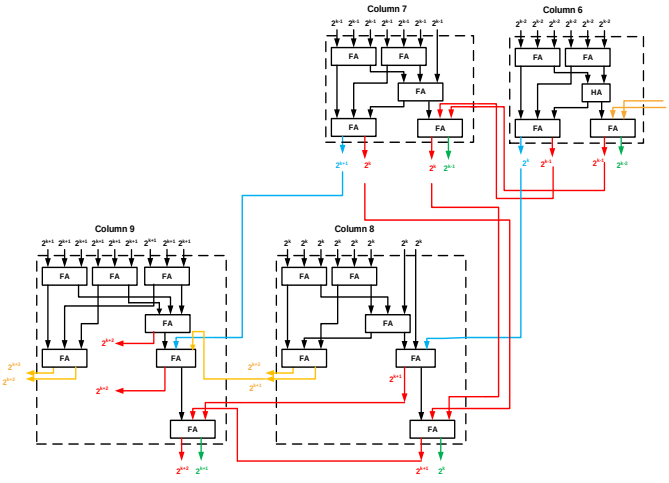
$$\sum \text{Input Weights} = \sum \text{Output Weights} \quad (2)$$
$$9*2^{K} = 2^{K} + 2^{K+1} + 2^{K+1} + 2^{K+2}$$
$$9*2^{K} = 9*2^{K}$$

C. Discussions: Performance Analysis on Cascade Models

High order (8:2) and (8:3) compressors are used for partial product reduction [12]. So, they can reduce 8 rows of partial products into two and three rows.
Fig.3 shows how 4 columns out of the 6,7,8 and 9 rows of partial product array are reduced by (6:2), (7:2), (8:2) and (9:2) compressors in 16*16-bit multiplication process.



3.a: Cascaded (n:2, 6≤n≤9) Compressors in 16*16-bit Multiplier



3.b: Conventional Structure of (n:2, 6≤n≤9) compressors in parallel mannaer

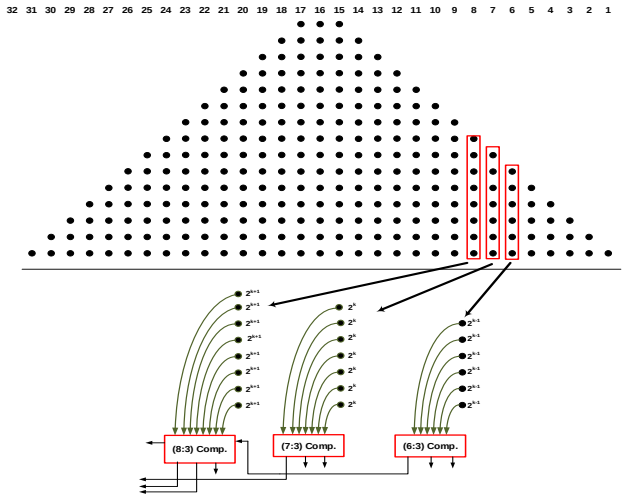
Figure 3. cascaded (n:2, 6≤n≤9) compressors in parallel mannaer

To enhance the performance, all carry-in(Cin) signals must be valid if needed to optimize all mentioned compressors. Considering 8th column (Fig. 3) with three

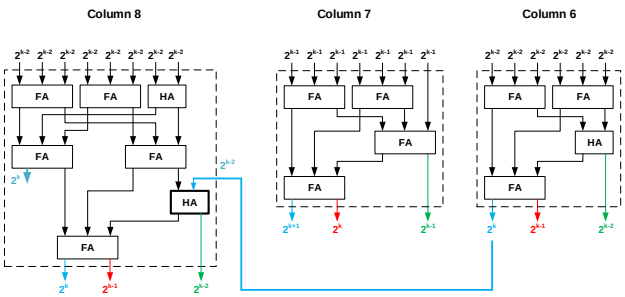
(Cin). The first carry-in signal comes from one of the carry-out signals of the 6th coloumn and the two last carry-in signals come from the 7th coloumn.

In this case, if all the inputs employed to all four compressors at time τ_0, the delay of the (8:2) compressor is not just the delay of four Full Adder (FA) cells. Since the fourth FA cell of the (8:2) compressor needs all the three input signals at time $\tau 2$, one of the signals would be available at time $\tau 3$ so, the (8:2) cascaded compressors would tolerate delayed signals from its neighbor and delay increase. Moreover, the last FA cell in (8:2) compressor must tolerate the delay of two carry-in signals because these two carry signals come from the 7th coloumn which are must be valid at $\tau 3$ but they are valid at $\tau 4$.

Accordingly, suppose the same scenario for three cascaded (n:3, 6≤n≤8) compressors. If all the inputs employed to all three compressors at time τ_0, the mentioned problem for the (8:3) compressor do not exist because the only carry-in signal which is come from the 6th coloumn would be valid at $\tau 3$ and there is no dependency between coloumn 7th and 8th cascaded models (Fig.4).



4.a: Cascaded (n:3, 6≤n≤8) Compressors in 16*16-bit Multiplier



4.b: Conventional Structure of (n:3, 6≤n≤8) compressors in parallel mannaer

Figure 4. cascaded (n:2, 6≤n≤8) compressors in parallel mannaer

III. Simulation Results Analysis And Comparison

Three accepted metrics to measure the quality of a digital circuit are: delay, power and area. Besides, for evaluating the performance of logic gates and having cost effectiveness circuits, designers must consider both design perspective and technology perspective. Althought MOSFET technology has been the best solution for miniaturization and optimization of chip-level gates[ajse], but according to ITRS (International Technology Roadmap for Semiconductor), silicon transistor will reach to its minimal limit by 2021[14] due to fundamental drawbacks such as such as short-channel effects, high leakage power dissipation, large parametric variations. Emerging nanotechnology will improve the semiconductor industry [15]. CNFET is one of the most promising devices among emerging technologies because of its inherent similarities to the current technology (CMOS), so designers should be considered about designing the future generation of integrated circuits based on its superior properties [16].

In this section, two adders are deployed based on CNFET technology in order to make a fair technology-independent comparison, and also to conduct a survey of future technology impacts on both (8:2) and (8:3) compressors architecture designs.

A. *Symmetric Full-Adder Circuit Design*

The 30T transistors Carbon Nano-Tube Full-Adder (CNTFA) cell is selected as the Full-Adder cell for the comparison due to its high performance and novel structure[17]. The design take advantage of low energy consumption and fully symmetrics structures. Moreover, with the purpose of decreasing the number of transistors, and in a built-in manner, all the all the complementary inputs are produced inside the circuit (Fig.5).

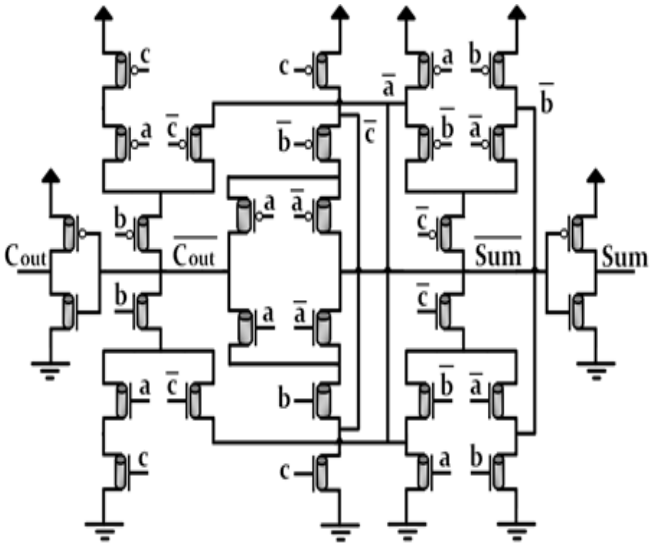


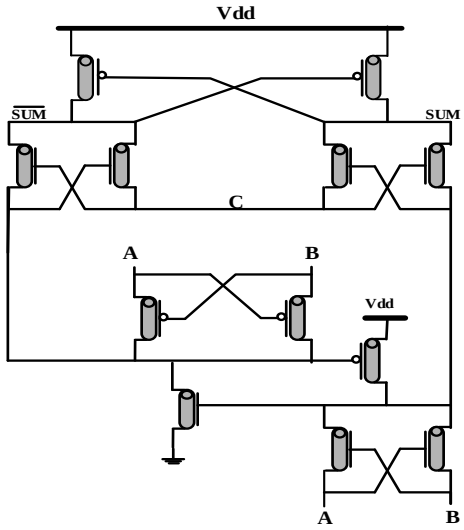
Figure 5. Symmetrical Full-Adder Cell design[17]

According to Fig.5, the proposed circuit integrate the Sum and C_{out} to design a unit structure Full Adder cell.

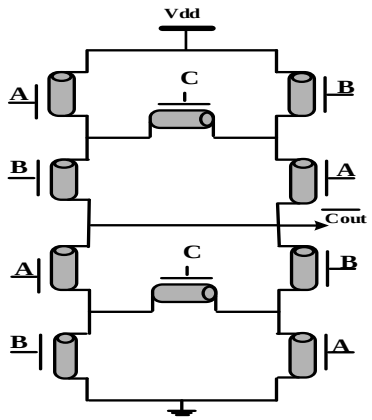
The integration process leads to elimination of overhead transistors which results in less power dissipation and occupied area, without performance degradation. It benefits from high driving power, symmetry and mirror input pattern characteristic which lead to simple fabrication process. The whole adder cell is considered as a fully indirect Full Adder structure.

B. Hybrid Full-Adder structure

The low-power, high-speed and high-performance 24T transistor 1-bit hybrid Full Adder cell(Fig.6), uses two XOR/XNOR modules to create the Sum signal.[18]



6.a : First stage (sum)



6.b: Second stage (Cout)

Figure 6. Hybrid Full-Adder Cell design[18]

According to Fig. 6, the great advantage of this hybridization, is that although the second stage needs an inverted input signal, the existence of the intermediate XNOR output, produced by the first stage, leads to elimination of the extra inverter gate. As a result, this elimination leads to a shorter critical path and accordingly shorter worst-case delay and also lower power consumption and occupied area. Therefore, the proposed adder cell is a combination of XOR/XNOR circuits to achieve a veryhigh-performance Sum generator.[17]

C. Simulation Results

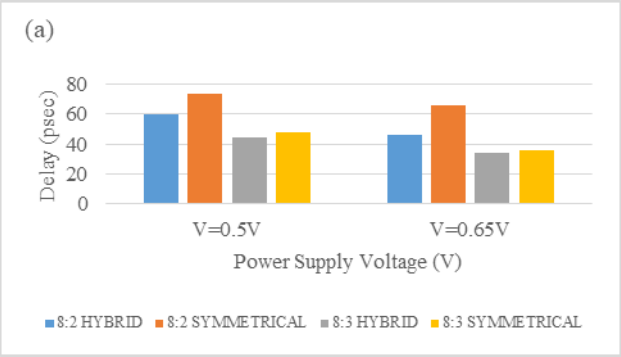
Since digital circuits at the heart of electronic device need to dissipate low power in order to conserve battery life and meet reliability constraints, lowering power consumption is the key of design not only for lengthening battery life in portable device but also for improving reliability in robust, fault-tolerant and low-power systems. Moreover, in today's VLSI circuit design, with scaling down the feature size of devices in nanoscale and the continuous decrease in the threshold voltage, the ability of operating with high performance at low power supply are highly in demand.

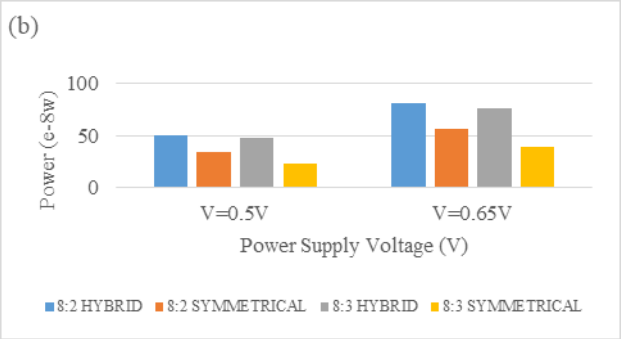
The number of nanotubes and the values of pitches of CNFETs are set suitably with the aim of minimizing the power-delay product, based on the transistor sizing procedure of [19-20] (Table I).

TABLE I. CNFET MODEL PARAMETERS

Parameter	Description	Value
L_{ch}	Physical channel length	32nm
L_{geff}	The mean free path in the intrinsic CNT channel	100nm
L_{ss}	The length of doped CNT source-side extension region	32nm
L_{dd}	The length of doped CNT drain-side extension region	32nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4nm
C_{sub}	The coupling capacitance between the channel region and the substrate	20pF/m
Efi	The Fermi level of the doped S/D tube	6eV

To evaluate this capability, simulation results shown in Fig. 7(a), 7(b) and 7(c), ease the comprehensive comparisons. In this experiment, both (8:2) and (8:3) compressor circuits have been simulated at both 0.5V and 0.65V power supply voltage. Simulation results , based on Synopsys HSPICE with 32nm CNTFET technology ease the comprehensive comparisons. In this experiment, the (8:3) compressor based on symmetrical Full-Adder design demonstrate the superiority of the design in terms of power, delay and PDP, specifically at 0.5v supply voltages. It can be discovered from Fig. 7 the (8:3) compressor based on the symmetrical Full-Adder cell design has the lowest power and power-delay product (PDP) at 0.5v power supply.





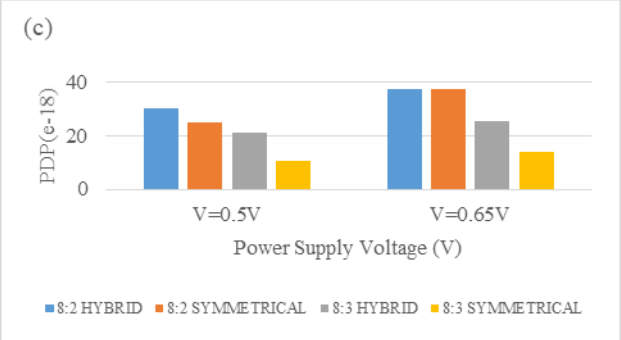


Figure 7. Simulation results

IV. Conclusion

Compressors are widely used in the second phase of a multiplier to accumulate partial products in a concurrent manner. They are mostly used in multipliers to reduce the operands while adding terms of partial products. In this paper we have carried out a comprehensive analysis and comparison between two different (8:2) and (8:3) compressors by deploying two recent Full-Adder cell designs based on CNFET technology and compare them at the transistor level. Based on the experimental results, the three carry input signals in (8:2) compressor architecture cause extra interconnections, more power dissipation, coupling effects, and routing difficulties. As a result, the (8:3) compressor consumes less power compared to (8:2) compressor. Furthermore, it is even more efficient (Considering PDP) than its counterpart.

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Shima Mehrabi was born in Tehran, Iran, in 1981. She received the bachelor's degree in hardware engineering from the South Tehran Branch, IAU, Tehran, in 2004, and the master's and Ph.D. degrees in computer architecture from the Science and Research Branch, IAU, Tehran, in2007 and 2013, respectively. Her current research interests include nanoelec-tronics with emphasis on CNFET, computer arith-metic, and very large scale integration design.

Amirhossein Jamalian received the bachelor's degree in computer engineering from the South Tehran Branch ,Islamic Azad University, Tehran, Iran in 2004, and the master's degree in computer engineering from the Sharif University of Technology, Tehran, in2007. From 2009 to 2013, he was a Full-Time Faculty Member with Andisheh Branch, Sama Organization, Islamic Azad University. He is currently a Ph.D. candidate in artificiall intelligence with the Depart-men tof Computer Science, Chemnitz University of Technology, Chemnitz, Germany. His current research interests include computational neuroscience, machine/robotvision, objectrecognition, and machine learning