A Novel Method of CoW Bonding for High Density Ultra-Fine Pitch IC Stacking Application

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***Abstract*—CoW (chip on wafer) Cu-Cu low temperature <200 ℃ process is developed for 3D IC stacking application. The CoW process includes chip tacking and global bonding. The bottleneck and challenges are (1) preventing chip shifting during global bonding, (2) Cu height uniformity, (3) reducing bonding temperature and force. A 3D IC with high density I/O test vehicle is designed and demonstrated the low temperature Cu-Cu interconnects application. C2W bonding approach is used for the 3D IC stack bonding method and is found suitable for devices with TSV structure. A novel approach by using Sn electroless plating solution as temperature tacking agent achieved good CoW bonding. It is found that no chip shifting in global bonding. At same time, the bonding force is also reduced from 800N/chip to 100N/chip with bonding temperature at 200 ℃. Final cross section of bonded sample showed good joint without void.**

***Index Terms*—CoW bonding, Cu-Cu, High density I/O, DRAM**

I. Introduction

Electronics packaging industry constantly demand for fine pitch flip chip bonding technologies to support lesser thickness, smaller form factor, higher operating frequency, lower power consumption, and lower manufacturing cost for next generation communication devices, 3D memory stacks and CMOS image sensor (CIS) packaging. Increase of functionality of devices drives for a larger number of I/O counts requirement while decrease of transistor size drives for fine pitch interconnects requirement. With the decrease of bump size and pitch, the bonding methodology changed from solder ball to Cu pillar to Cu-Cu bonding. Cu pillar with solder cap has successfully replaced solder bump nevertheless it has found its technical limitations below 30μmpitch that spreading solder bridges neighboring Cu pillars (Fig. 1). Cu-Cu diffusion bonding nicely fit into the region below 20 micron pitch and has demonstrated by several works (Fig. 2) as reported in [1]-[4].

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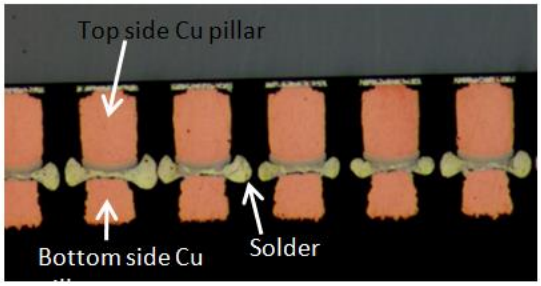

Figure 1. Bridging solders during thermo-compression bonding. (Cu pillar diameter: 15 um)

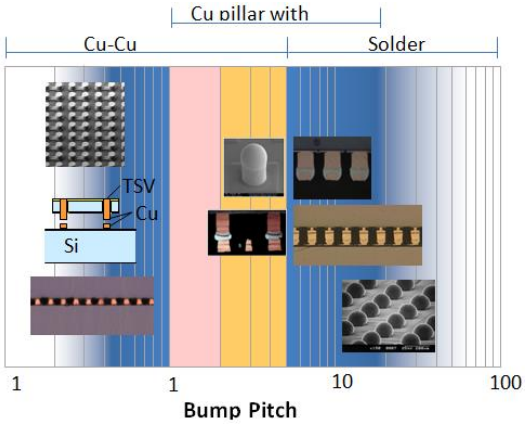

Figure 2. Bump pitch versus bonding methods

However, Cu-Cu bonding itself has its own limitations due to requirements of higher bonding temperature (over 350 ℃), higher-bonding force and longer bonding time (over 30 min per bonding). Higher temperature limits the number of applicable devices, higher bonding force may damage the devices, particularly those integrated with low-k dielectrics, and longer bonding time lowers the throughput limiting commercial production. Accordingly, improving these three parameters is an essential requirement in realizing 3DICs with high-density interconnect bonding and bring that technology into mainstream production.

In mass production, it is not economic to do C2C (Chip to Chip) Cu-Cu bonding as it takes long bonding time to form joint. CoW bonding can greatly improve the through put. The other important fact is most of the 3D IC integration need CoW bonding as the chip sizes are different. However, most of the work reported to date is on wafer-on-wafer bonding technology.

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CoW bonding technique has been studied in industry for a few years [5], [6]. One of the bottlenecks is the chip shifting during global bonding. This paper will introduce a novel approach to solving this key issue in CoW bonding for high density I/O interconnects and reduce bonding temperature.

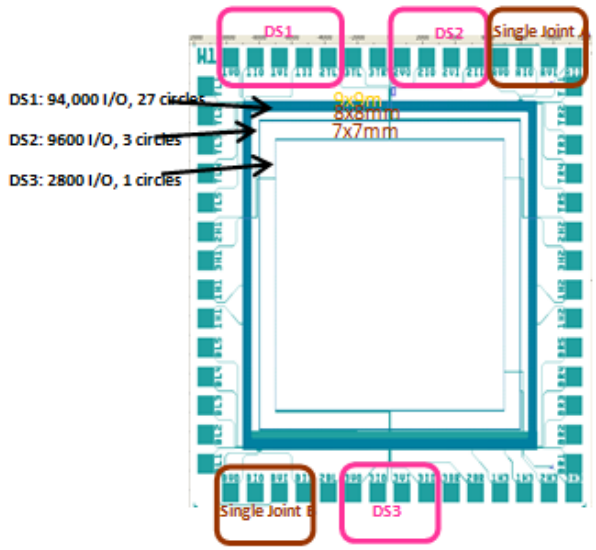

Figure 3. Layout of test vehicle designed. (Three different daisy chains having 98K, 9.8k and 0.98k interconnects patterns were fabricated on each chip)

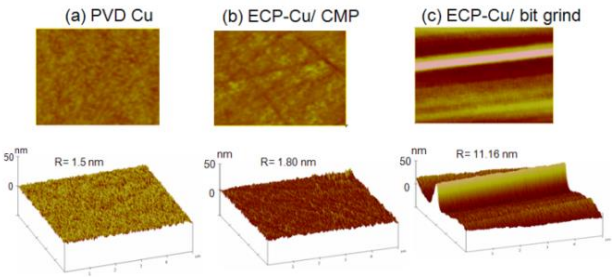

Figure 4. Surface roughness of Cu surfaces prepared by (a) as deposited PVD film, (b) CMP film and (c) bit-grinded

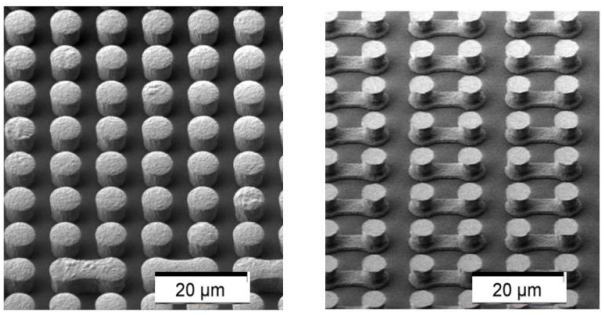

Figure 5. DR-SEM image of Cu pillar array (a) before and (b) after planarization

II. Test Vehicle Design and Fabrication

High density micro-bumps test vehicles are design and fabricated. There are a top chip and a bottom wafer. Once the top chip and bottom wafer are aligned and bonded, three daisy chains will be connected. They are composed by the Cu pillar at outer rings of the chip, middle and center rings with 94K, 9.6K and 2.8K interconnects respectively. (Fig. 3)

Both top and bottom wafers are fabricated on 300mm silicon wafer. For the top chip, wafer is first deposit a layer of silicon oxide. Or polyimide is coated on wafer as passivation layer. Then the dia7um and pitch 10um RDL layer is pattern and electroplated on silicon oxide. As 2nd metal layer, the diameter 5um and pitch 10um copper pillars are patterned and electroplated on top of RDL layer. Within 10mm x 10mm top chips size, the Cu pillar density is 106/cm2. Without removing photo resist, the wafer goes through planarization step to flatten the surface and get all Cu pillars uniform height. The height of Cu pillar is planarized to 4μm by bit-grinding process. Fig. 4 shows the surface roughness comparison among bit PVD copper, copper after CMP (chemical mechanical polish) and bit grind. Data shows the bit grinded Cu surface is rougher than CMP surface, but bit grind process is economically more production worthy [7]. The first photo in Fig. 5 shows the Cu pillar array after electroplating. The pillar tip has nature dome shape. The 2nd photo shows after bit grinding, the Cu pillar is planarized with flat surface. The fabricated wafer has high density Cu pillars with uniform height. (Fig. 5)

With the same method, the bottom wafer with the same pitch and 7um diameter RDL is also fabricated. The RDL links to probing pads, located at peripheral area of bottom die. As the bottom wafer RDL thickness is only1um thick, the wafer cannot process bit grinding. The die size on bottom wafer is 12x12mm.

III. CoW Aseembly

In this study, a novel assembly method is used for Cu-Cu bonding. The process flow is listed in Fig. 6. As a preparation step, a thin layer (~500nm thick) Sn electroless plating solution is spin coated on a blanket tray.

The top chip is diced and ready to use. The Cu pillar and Cu RDL on top chip and bottom wafer already oxidize immediately after fabrication, the copper oxide is an obstacle for Cu-Cu bonding. Therefore, known good chips and bottom wafer are deoxidized to remove copper oxide before assembly [7]-[9].

Flip chip bonder is used for chip pick and place. The bonder arm pick up top chip, then stamp on the Sn electroless plating solution. As the solution is only 500nm, while the Cu pillar has height of 4um, the solution only wet Cu pillar tip surface. The chip is then moved to wafer top for alignment, finally mount on bottom wafer. The plating solution is function at 60 ℃ to grow Sn layer on top of Cu. So the bottom wafer maintains at 60 ℃ by flip chip bonder's bottom chuck. When the top chip touches the bottom wafer, the solution on Cu pillar tip gets heated and a thin layer of Sn starts growing on bonding interface. As solution is getting contact with both bottom wafer pad and top chip Cu pillar, so the Sn layer grows on both sides and make a joint. The thin Sn joint is not strong, but the strength is sufficient to acts as temporary adhesive to hold chip position firmly while transferring sample from flip chip bonder to global bonding process and

throughout gang bonding process. The Sn layer also smoothes the Cu pad surface topography on bottom wafer, which is not able to process bit grinding during bottom wafer fabrication. The tacking process does not need to use high force, as the Sn plating is chemical process. Repeat the tacking step underfill, the top chips are aligned and positioned on whole wafer.

The sample is then sent to gang bonder. The wafer is placed on bottom stage. All the chips are pressed down and then heated up for more than 15mins. All the joints are formed at same time. Global bonding temperature and force are 200 ℃ and 100N per chip, respectively.

In mass production, heating and cooling is most time consuming. Compare with assembly chip one by one (heat up and cool down many times on one wafer), CoW with above two steps only heat and cool the whole wafer once, so the throughput is much higher. As the Cu pillar diameter is only 5 um, flip chip bonder with high-precision alignment accuracy is used.

To keep chip position fixed during global bonding is a challenge. The global bonder piston is full wafer size. When the piston presses down, it gets contact with chips top surface. Chip shifting could take place due to chip thickness variation, non-uniform force distribution among chips and high bonding force. For low temperature Cu-Cu directly bonding, high force is needed. However, it becomes one reason of chip shifting due to chip sliding. Many researches are on-going to solve chip shift issue. In this study, a novel approach is used by applying a layer of Sn electroless plating solution as adhesion agent.

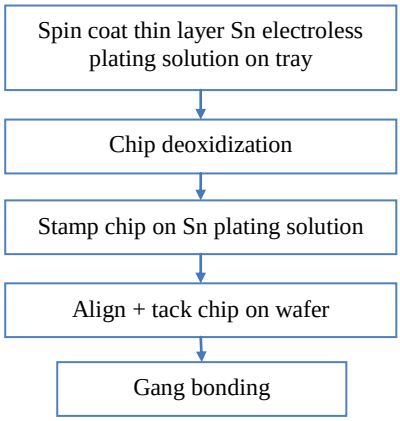

Figure 6. Process flow of assembly

IV. Results

High density Cu-Cu interconnects is realized at 200 ℃ with a bonding force of 100N/chip (Fig. 7). No chip shifting is observed in CoW bonding process. Cross section result shows no voids or unbounded contacts in joint.

As comparison, Cu-Cu bonding without using Sn electroless plating solution is also studied. It is noticed that bonding force has great relation with Cu surface condition. Bit grinded Cu pillar needs 800N/chip bonding force. However, under 800N bonding force, the polyimide layer beneath Cu pad generates cracks and delaminates from Si surface (Fig. 8). Also, due to the higher bonding force, the surface RDL are found to bend.

After using Sn electroless plating solution and process introduced in this paper, the bonding force is greatly reduced. In Gang bonder, using small piston force can help to reduce chip shifting due to sliding. Small bonding force also benefits the whole structure reliability by reducing plastic deformation of the RDL and polymeric underlayer with successful Cu-Cu bonding achieved.

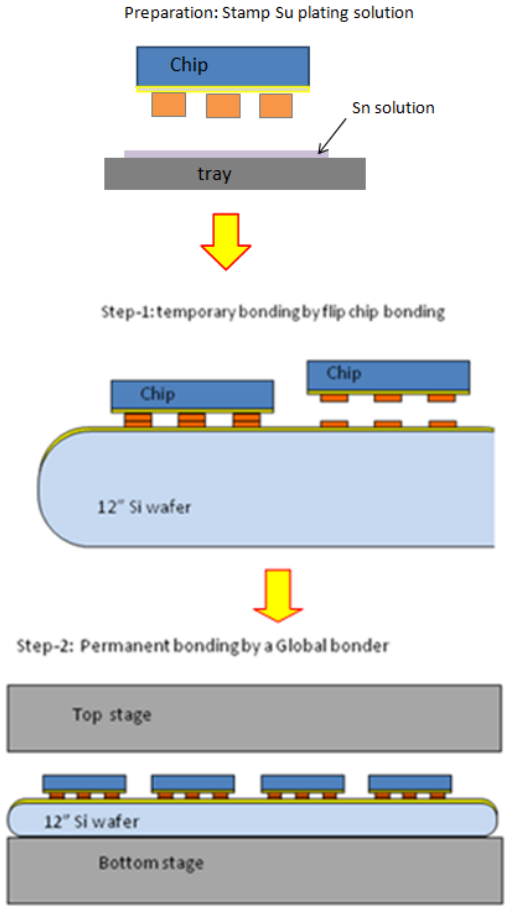

Figure 7. Two step bonding process. In the preparation, the chip was stamped on Sn electroless plating solution, in the first bond step temporary bonding with flip chip bonder is carried out. In the second step permanent bonding with a global bonder is carried out.

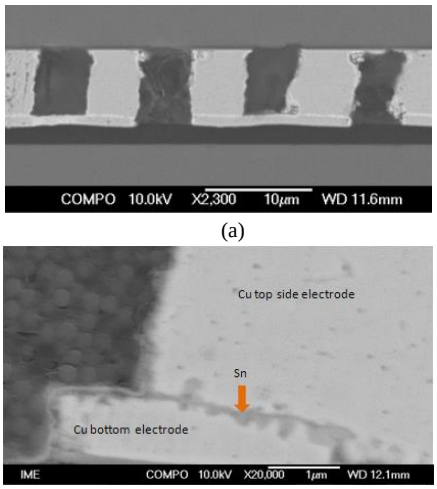

Figure 8. Cu-Sn-Cu cross section (a) Cu pillar bonded to bottom wafer (b) bonding interface

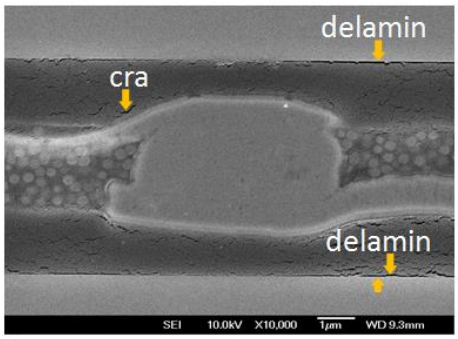

Figure 9. Without Sn electroless plating solution, cracks of polymer layer after Cu-Cu bonding with high bonding force

V. Summary

A novel method of CoW bonding is introduced. With the established process, high-density Cu-Cu interconnects with density over 106 interconnects/cm2) is realized. Improving surface uniformity of Cu pillar and removing surface oxide facilitate reducing Cu-Cu bonding temperature to 190℃. Application of electronics Sn solution as tacking agent at the bond interface lowers the bonding force up to 100 N. The CoW bonding procedure helps in improving the Cu-Cu bonding throughput. Applicability of this high density bonding for CIS and Digital Signal Processing (DSP) integration are being studied.

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